In the Claims:

Please add the following Claims:

SUB C2 7

21. The method according to Claim 17 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

B1

22. A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;

a liner oxide layer overlying said polysilicon traces;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped profile; and

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

23. The device according to Claim 22 wherein said liner oxide layer has a thickness of between about 50 Angstroms and 300 Angstroms.

24. The device according to Claim 22 wherein said interlevel dielectric layer comprises a combination material from the group of: TEOS undoped oxide, boron phosphosilicate glass (BPSG), undoped silicon dioxide, silicon nitride, and silicon oxynitride.

B1 Cont.

25. The method according to Claim 22 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

SUB C3

26. A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;

a liner oxide layer overlying said polysilicon traces;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped

profile and wherein said silicon nitride layer is formed by chemical vapor deposition; and

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

27. The device according to Claim 26 wherein said liner oxide layer has a thickness of between about 50 Angstroms and 300 Angstroms.

B1

28. The device according to Claim 26 wherein said interlevel dielectric layer comprises a combination material from the group of: TEOS undoped oxide, boron phosphosilicate glass (BPSG), undoped silicon dioxide, silicon nitride, and silicon oxynitride.

REMARKS

Examiner F. Erdem is thanked for the thorough examination and search of the subject Patent Application. Claims 21-28 have been added.